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Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2019.2922687

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Do, D-T., Nguyen, M-K., Quach, T-H., Tran, V-T., Blaabjerg, F., & Vilathgamuwa, M. (2020). A PWM Scheme for a Fault-Tolerant Three-Level Quasi-Switched Boost T-Type Inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, *8*(3), 3029-3040. [8736357]. https://doi.org/10.1109/JESTPE.2019.2922687

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A PWM Scheme for a Fault-Tolerant Three-Level Quasi-Switched Boost T-Type Inverter

Duc-Tri Do, Minh-Khai Nguyen, *Senior Member, IEEE,* Thanh-Hai Quach, Vinh-Thanh Tran, Frede Blaabjerg, *Fellow, IEEE,* and Mahinda Vilathgamuwa, *Senior Member, IEEE*

***Abstract*—In this paper, a new optimal pulse-width modulation (PWM) scheme for a three-level quasi-switched boost T-type inverter (TL qSBT^{2}I) under normal and failure modes is proposed. The proposed method reveals its semiconductor fault tolerance capability in open-circuit fault condition situations as described in the paper. The PWM control algorithm for the fault-tolerant qSBT^{2}I is implemented by selecting appropriate values for the modulation index, shoot-through (ST) duty cycle and duty cycles of two additional switches. The steady-state analysis and operating principles of the fault-tolerant qSBT^{2}I are presented. A laboratory prototype was built to verify the operating principles of the qSBT^{2}I with the proposed modulation scheme before and after fault conditions.**

***Index Terms*—Fault tolerance, Z-source inverter, multilevel inverter, boost inverter, shoot-through, single-stage.**

I. Introduction

Multilevel voltage source inverters (VSIs) are increasingly used in power distribution systems presently since they allow efficient DC/AC conversion for grid connection. Multilevel VSIs provide benefits such as better quality power supply, reduced voltage stress on semiconductor devices and smaller filter size [1], [2]. For example, three-level (TL) VSIs are commonly applied in photovoltaic (PV) systems, STATCOM systems, uninterruptible power supplies (UPS), motor drives, and wind turbines [3]-[6]. In fact, traditional TL VSIs belong to a family of step-down converters since their peak output phase voltage is less than the input DC-link voltage. Additional boost DC-DC converters [7]–[11] are often used in VSIs to boost the input DC voltage to a desired AC output voltage in a two-stage power conversion process. However, shoot-through (ST) mode, where upper and lower switches in a leg are triggered simultaneously, is not allowed in the two-stage VSIs because of the danger in short-circuiting the DC source. In [12], the power switch failure is overcome by using bidirectional devices and fuses to reconfigure the converter topology. In [13], a TL active neutral-point-clamped (NPC) inverter is presented to keep the neutral-point voltage balanced and to obtain a continuous output voltage under semiconductor fault situations of short-circuit switch (SCS) and open-circuit switch (OCS). In spite of this, an SCS fault must be avoided because an abnormal short circuit will damage the device. In [14], an extra phase inverter leg is used to offer a hardware backup when any switch of the T-type inverter is faulty. Furthermore, the three phase legs of the T-type inverter can share overload current by adding this additional phase leg.

To address the disadvantages of the conventional TL inverter, the TL Z-source NPC inverter is presented in [15] with a combination of the merits of the Z-source network and TL inverter. A space-vector modulation technique is also introduced in [15] to improve the voltage transfer gain with minimized switching loss. However, the Z-source network uses a large number of passive components that increase the weight, size, and loss of the inverter system. Lately, many researchers have developed the quasi-switched boost inverter (qSBI) [16] to reduce the use of passive elements while retaining the advantages of the impedance-source inverters such as ST immunity, buck-boost voltage capability, and single-stage power conversion. Compared to the Z-source inverter, the work in [16] uses more active switches but less passive components. The qSBIs have been applied to the TL T-type inverter as presented in [17] with the following features as 1) reduced input current ripple, 2) high voltage gain, and 3) fixed and high modulation index as much as possible.

Stability and reliability of inverters are important in power distribution systems such as UPS, high-power medical instruments, and grid-connected renewable energy conversion systems [18], [19]. In these topologies, numerous cases of faults that can occur during the operation of the inverter are investigated. In fact, switching device faults are usually classified as either a SCS fault or an OCS fault. The SCS fault can appear owing to several causes like over-voltage, wrong gate drive signals, and over-temperature. The OCS fault commonly occurs because of the thermal cycling, loss of the gate drive signal and excessive collector current [20]. When compared to OCS failure, the SCS failure is not sustainable because of the unusual over current, which can destroy devices

Manuscript received January 25, 2019; revised April 12, 2019 and May 19, 2019; accepted May 29, 2019. (Corresponding author: Minh-Khai Nguyen).

D. T. Do, T. H. Quach and V. T. Tran are with the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam (e-mail: tridd@hcmute.edu.vn, haiqt@hcmute.edu.vn, and tranvinhthanh.tc@gmail.com).

M. K. Nguyen and M. Vilathgamuwa are the School of Electrical Engineering and Computer Science, Queensland University of Technology, 2 George Street, Brisbane 4000, Australia (e-mail: nmkhai00@gmail.com, mahinda.vilathgamuwa@qut.edu.au).

F. Blaabjerg is with the Department of Energy Technology, Aalborg University, Aalborg 9100, Denmark (e-mail: fbl@et.aau.dk).

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within a very short time. For that reason, both SCS fault diagnostic methods and the fault-tolerant control are implemented using hardware circuits [21], [22]. Although the OCS faults are not difficult to handle as compared to SCS faults, they will degrade the power quality of the inverter where output current distortion, noise, and vibrations are apparent. Therefore, numerous research efforts have been conducted for failure detection methods and fault-tolerant control [23]-[29]. In [23], an OCS fault diagnostic method determines the location of the faulty switch and the faulty clamping diode of an NPC inverter without using any hardware or complex computations. The performance of the T-NPC inverter is significantly improved by applying the fault tolerance algorithm when an OCS fault occurs. This method does not require any redundant legs and complex calculations [24]. To maintain the output voltage, a dual Z-source inverter under semiconductor failure modes is introduced in [25] with the elimination of common-mode voltage. On the other hand, a fault tolerant TL quasi Z source T-type inverter (qZST^{2}I) is studied in [26] with a large number of passive components. The fault-tolerant TL qZST^{2}I is operated by only changing the modulation scheme after the semiconductor fault without the need of redundant legs or complex calculations. Moreover, by using switched-boost cells in [16], the inverter topology in [27] is able to ride through the fault with the healthy inverter leg switches in OCS failure mode to maintain a balanced rated output voltage through changing the modulation scheme. However, the transient-current in the OCS failure mode is not described in [27]. In addition, the experimental results of the fault-tolerant TL boost inverter given in [27] are not comprehensive as only steady-state waveforms are shown. The modulation techniques for fault tolerance in [26] and [27] have the disadvantages in the fault mode that the inverter operates with a larger ST duty ratio and high inductor current ripple. Because of using large ST duty cycle (D), the modulation index (M) of the TL T-Type inverter is reduced with increased output distortion and voltage stress on devices. The deployment of Z-source inverter allows power supply stage to withstand severe short-circuit conditions as described in [28]. Another study on three-level dual Z-source inverters for fault tolerant applications is proposed in [29]. This topology consists of two cascaded Z-source inverters where inverters operate in normal mode under healthy conditions and they will resort to two-level operation when one of the inverters is faulty.

In this paper, operating principles, circuit analysis, and PWM control techniques before and after OCS fault modes for the TL qSBT^{2}I are presented. The fault-tolerant TL qSBT^{2}I is an amalgamation of quasi-switched boost networks with a TL T-type inverter which can operate before and after semiconductor failure modes effectively. The fault-tolerant TL qSBT^{2}I with the proposed PWM control algorithm does not require an additional phase leg to ride through OCS faults. When a semiconductor fault occurs, the inverter is simply reconfigured by redefining the modulation strategy. In addition, a flow chart to obtain the optimal parameters of the modulation index and the duty cycles is presented. Moreover, an analysis of the TL qSBT^{2}I topology in case of a failure of the boost switch in the impedance network has been carried out and analysis and simulation results reveal that the inverter would be able to ride through such a fault effectively. The proposed methodologies are verified using PSIM simulation results and performing experiments in a laboratory prototype. The fault-tolerant TL qSBT^{2}I with the proposed modulation scheme is reliable. It is also efficient when compared to similar fault tolerant impedance source converters in [26], [27]. Therefore, it can be readily applied in industry applications such as in PV power systems and motor drives.

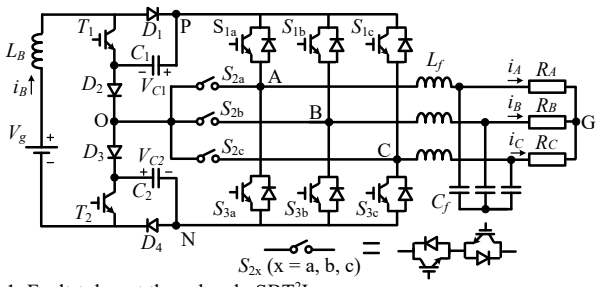

Fig. 1. Fault-tolerant three-level qSBT^{2}I.

II. TL qSBT^{2}I Topology Under Semiconductor Failure Modes

Fig. 1 shows the circuit topology of the fault-tolerant TL qSBT^{2}I. In the fault-tolerant TL qSBT^{2}I, an active impedance-source (AIS) network comprised of a boost inductor (L_B), two capacitors (C_1, C_2), two active switches (T_1, T_2), and four diodes (D_1–D_4) is employed and its output is then connected to a conventional T-type inverter, where six unidirectional switches and three bi-directional switches are used. The common connection point of the AIS is connected to three bi-directional switches S_{2a}, S_{2b}, and S_{2c}. One of the special features of this study is the introduction of some fault-tolerant capabilities of the topology when a power switch in the T-type inverter or in AIS is failed. As presented in [17], the fault-tolerant TL qSBT^{2}I in the normal mode has two main states: shoot-through (ST) and non-shoot-through (NST). In the ST state, all switches S_{ix} (i = 1, 2, or 3; and x = a, b, or c) of the T-type bridge circuit are turned on at the same time, whereas both switches T_1 and T_2 are turned off. The inductor stores energy in the ST state, while the capacitors are idle. In the NST state, the T-type inverter side is equivalent to a current source, whereas the charged and discharged states of the capacitors and inductor depend on the turn-on and turn-off states of switches T_1 and T_2.

A. Operating Principle of TL qSBT2I under Fault Mode

The fault-tolerant operation of TL qSBT^{2}I can be divided into three cases: S_{1x} or S_{3x} failure, S_{2x} failure (x = a, b or c), and T_1 or T_2 failure. Fig. 2 presents two phase-A fault modes. Fig. 3 shows the reference voltage vectors of the inverter in normal operation ($\overrightarrow{V_a}$, $\overrightarrow{V_b}$, and $\overrightarrow{V_c}$) and in fault operation ($\overrightarrow{V_a'}$, $\overrightarrow{V_b'}$, and $\overrightarrow{V_c'}$). When a fault in S_{1x} or S_{3x} occurs, the reference voltage vectors of the inverter must be modified to $\overrightarrow{V_a'}$, $\overrightarrow{V_b'}$, and $\overrightarrow{V_c'}$ as shown in Figs. 3(b)-3(d). To maintain the output line-to-line voltage at the pre-fault value, the phase angle of reference vectors $\overrightarrow{V_b'}$, and

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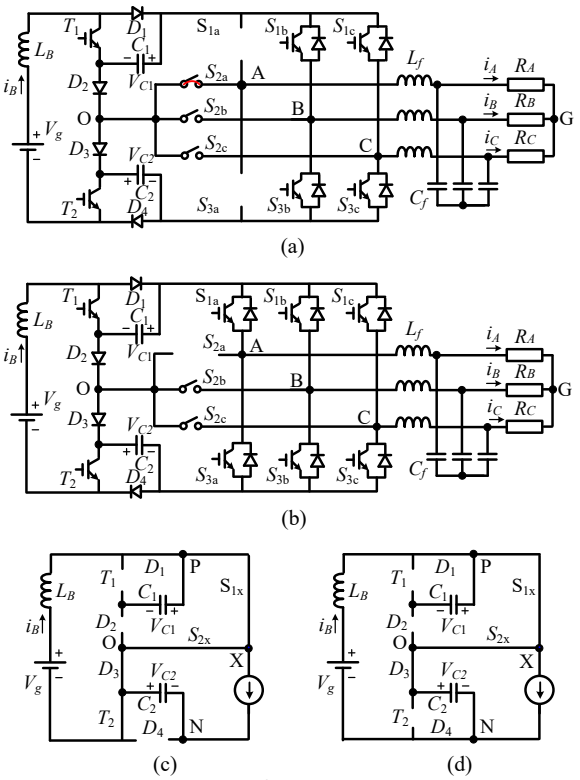

Fig. 2. Operating states of TL qSBT²I in semiconductor failure conditions. (a) S_{1a} or S_{3a} OSC fault, (b) S_{2a} OSC fault, (c) NST 5 state with OSC T_1 or T_2 fault, and (d) NST 6 state with OSC T_1 or T_2 fault.

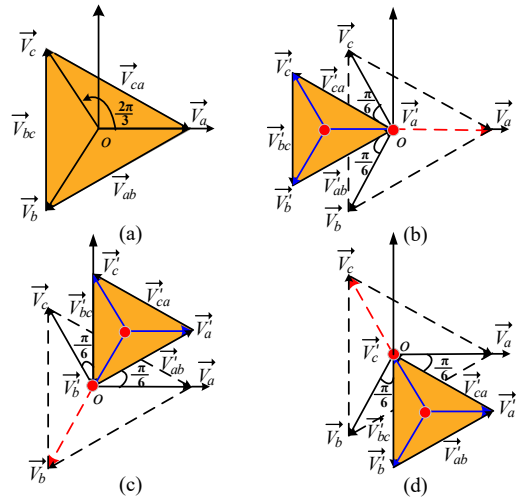

Fig. 3. Reference voltage vectors in (a) normal mode, (b) phase-A fault, (c) phase-B fault, and (d) phase-C fault.

TABLE I
CORRECTIVE ANGLES IN NORMAL AND FAULT CONDITIONS

Modulating signal	$\overrightarrow{V_a'}$	$\overrightarrow{V_b'}$	$\overrightarrow{V_c'}$	$\overrightarrow{V'_{ab}}$	$\overrightarrow{V'_{bc}}$	$\overrightarrow{V'_{ca}}$
Normal operation	0	-2π/3	2π/3	π/6	-π/2	5π/6
Phase A fault	0	-5π/6	5π/6	π/6	-π/2	5π/6
Phase B fault	π/6	0	π/2	π/6	-π/2	5π/6
Phase C fault	-π/6	-π/2	0	π/6	-π/2	5π/6

$\overrightarrow{V_c'}$ must be changed, while the amplitude of these reference vectors is unchanged. The reference voltage of the faulty phase is set to zero. Then, the amplitude of line-to-line voltage vectors ($\overrightarrow{V'_{ab}}$, $\overrightarrow{V'_{bc}}$, and $\overrightarrow{V'_{ca}}$) in the fault mode is reduced by $\sqrt{3}$ times compared to that in the normal mode with their phase angles unchanged. Table I shows the phase angle of the reference voltage vectors of the inverter in normal and fault conditions.

Case 1: Fault-tolerant control when S_{1x} or S_{3x} is faulty

If the OCS failure occurs in switch S_{1a} or S_{3a} in Fig. 2(a), the output phase-A voltage, V_{AO} is not able to produce either $+V_C$ or $-V_C$, which results in the load current asymmetrical and distorted. As a result, the faulty phase is used to maintain continuous output voltage by triggering middle-point switch S_{2a} while switches S_{1a} and S_{3a} are turned off. On the other hand, the reference voltage vectors $\overrightarrow{V_a}$, $\overrightarrow{V_b}$, and $\overrightarrow{V_c}$ are modified as described in Figs. 3(b)-3(d) to keep balanced line-to-line voltages. When phase-A operates in open-switch S_{1a} or S_{3a} fault mode, the reference phase angles of $\overrightarrow{V_b'}$ and $\overrightarrow{V_c'}$ are redefined as -5π/6 and +5π/6, respectively. Similarly, when the phase-B operates in open-switch fault mode, the reference phase angles of $\overrightarrow{V_a'}$ and $\overrightarrow{V_c'}$ are redefined as π/6 and π/2, respectively. Also, when the phase-C operates in open-switch fault mode, the reference phase angles of $\overrightarrow{V_a'}$ and $\overrightarrow{V_b'}$ are redefined as -π/6 and -π/2, respectively. As shown in Table I, the reference phase angles of line-to-line voltages before and after fault are unchanged with the application of new modulating signals [30].

Case 2: Fault-tolerant control when S_{2x} is faulty

If the OCS failure occurs at switch S_{2a}, the output pole voltage of the phase-A leg cannot be connected to the neutral point of the AIS network. To solve this issue in the most of the situations, switches S_{1a} and S_{3a} in the fault-tolerant TL qSBT²I is used to generate a two-level voltage for the phase-A leg, while the switches of the phase-B and phase-C legs are used to generate a three-level voltage for phase-B and phase-C legs as shown in Fig. 2(b). Then, the control variables are maintained as operating in pre-fault. However, the harmonic distortion of phase-A with two-level voltage is higher than that of phase-B and phase-C.

Case 3: Fault-tolerant control when T_1 or T_2 is faulty

When an OCS failure occurs at switch T_1 or T_2 of the switched boost network, capacitor C_1 and C_2 voltages are unbalanced. As a result, the output phase voltage and load current are distorted and their amplitudes are reduced. Suppose an OCS failure of T_1 occurs, the ST state of the T-type inverter and the control signal of T_2 need to be used to maintain the output voltage at its pre-fault level in the fault-tolerant TL qSBT²I. Figs. 2(c) and 2(d) show two new NST states of the inverter when the OCS T_1 fault occurs. To maintain the output voltage at its pre-fault value, switches S_{2x} and S_{3x} (x=a, b or c) are used to generate a two-level output voltage with a new DC-link between nodes O and N, while switch S_{1x} is used to charge capacitor C_2. The capacitor C_2 voltage is boosted to the DC-link voltage because capacitor C_1 is disconnected in this case. Then, only capacitor C_2 is used in the power circuit to produce the two-level output voltage of $-V_{C2}$ and 0. Therefore, the capacitor voltage balance does not arise under faulty mode of T_1 or T_2.

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B. Circuit Analysis for the Fault-Tolerant TL qSBT²I

The operating principle of the fault-tolerant TL qSBT²I is based on the switching states in Table II. Similar to the traditional TL ZSIs, the fault-tolerant TL qSBT²I under phase-A fault as shown in Figs. 2(a) and 2(b) can also operate in two main modes: NST and ST. Table II presents the operating modes of the fault-tolerant TL qSBT²I.

1) NST Mode

In the NST mode, the fault-tolerant TL qSBT²I generates three different voltage levels: $+V_C$, 0, and $-V_C$ by handling the switches of the T-type inverter. When S_{1x} ($x = b$ or c) is switched "ON" under phase-A fault condition, the pole phase voltage, V_{XO} is $+V_C$. If S_{2x} is switched "ON", the neutral point (node O in Fig. 1) is linked to the load, thus, V_{XO} is zero. When S_{3x} is switched "ON", V_{XO} is $-V_C$. The NST mode is classified into four submodels: NST 1, NST 2, NST 3, and NST 4.

In the NST 1 mode, switch T2 is switched "OFF", whereas switch T1 is switched "ON". Diodes D2, D3, and D4 are ON, whereas D1 is OFF. Capacitor C2 is charged, whereas inductor LB and capacitor C1 do not store energy. The inductor voltage is obtained as

$$L_B \frac{di_B}{dt} = V_g - V_{C2}. \tag{1}$$

In NST 2 mode, switch T_1 is switched "OFF", whereas switch T_2 is switched "ON". Diodes D_1, D_2, and D_3 are ON, whereas diode D_4 is OFF. Capacitor C_1 is charged, whereas inductor L_B and capacitor C_2 are discharged. The inductor voltage is defined as

$$L_B \frac{di_B}{dt} = V_g - V_{C1}. \tag{2}$$

In NST 3 mode, switches T_1 and T_2 are switched "ON". Diodes D_1 and D_4 are OFF, whereas diodes D_2 and D_3 are ON. Inductor L_B stores energy, whereas capacitors C_1 and C_2 do not store energy. The time interval in this mode is $D_0 \cdot T$, where D_0 is the ST duty cycle. The inductor voltage is defined as

$$L_B \frac{di_B}{dt} = V_g. \tag{3}$$

In NST 4 mode, switches T_1 and T_2 are switched "OFF". Diodes D_1, D_2, D_3, and D_4 are ON. Capacitors C_1 and C_2 store energy from V_g while the main circuit receives energy from inductor L_B. The inductor voltage is given as

$$L_B \frac{di_B}{dt} = V_g - V_{C1} - V_{C2}. \tag{4}$$

2) ST Mode

In this ST mode, switches S_{1b}, S_{1c}, S_{2b}, S_{2c}, S_{3b}, and S_{3c} in the T-type inverter are switched "ON" simultaneously, whereas switches T_1 and T_2 are switched "OFF" simultaneously. Diodes D_2 and D_3 are OFF, while diodes D_1 and D_4 are ON. Capacitors C_1 and C_2 have not transferred energy to the main circuit. This time interval is $D_0 \cdot T$. Inductor L_B stores energy from V_g. The inductor voltage is

$$L_B \frac{di_B}{dt} = V_g. \tag{5}$$

TABLE II
SWITCHING STATES OF FAULT-TOLERANT TL QSBT²I

Phase-*A* fault condition			
State	Triggered Switches	On Diodes	V_{BO} or V_{CO}
NST 1	T_1	D_2, D_3, D_4	$+V_C$, 0 or $-V_C$
NST 2	T_2	D_1, D_2, D_3	$+V_C$, 0 or $-V_C$
NST 3	T_1, T_2	D_2, D_3	$+V_C$, 0 or $-V_C$
NST 4	S_{1b}, S_{1c}	D_1, D_2, D_3, D_4	$+V_C$
	S_{2b}, S_{2c}		0
	S_{3b}, S_{3c}		$-V_C$
ST	S_{1b}, S_{1c}, S_{2b}, S_{2c}, S_{3b}, S_{3c}	D_1, D_4	0
Additional states under switch T_1 fault condition ($x = a, b, c$)			
NST 5	S_{1x}, S_{2x}, T_2	D_1, D_3	0
	S_{3x}, T_2		$-V_{C2}$
NST 6	S_{1x}, S_{2x}	D_1, D_3, D_4	0
	S_{3x}		$-V_{C2}$
ST	S_{1x}, S_{2x}, S_{3x}	D_1, D_4	0

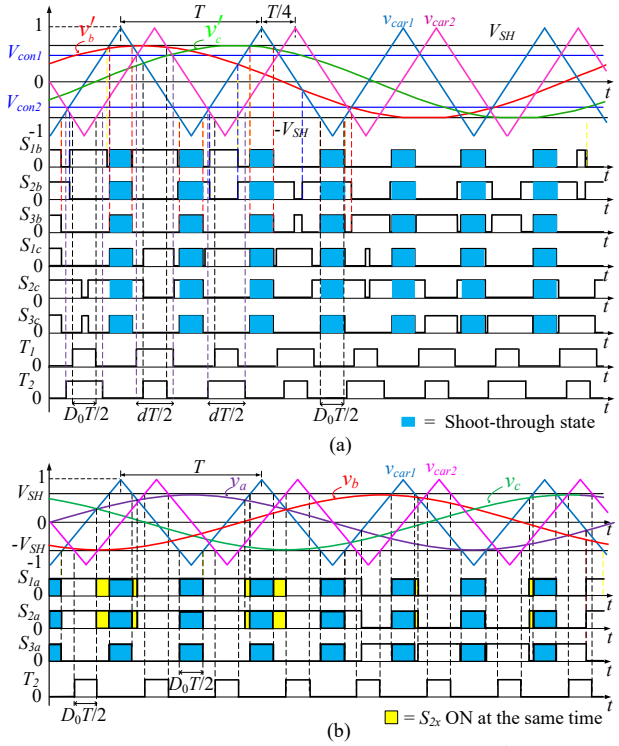

Fig. 4. PWM control method for the fault-tolerant TL-qSBT²I under conditions of (a) OCS S_{1a} or S_{3a} fault and (b) OCS T_1 fault.

C. PWM Control Method for the Fault-Tolerant TL qSBT²I

Fig. 4(a) shows the PWM control method for the fault-tolerant TL qSBT²I when a fault occurs in phase-A. In Fig. 4, V_{SH}, V_{con1}, and V_{con2} represent control signals of ST, T_1 switch, T_2 switch, respectively. To control the three-phase load voltages after the fault occurrence, the reference voltages of the inverter are modified as shown in Fig. 3(b). The reference voltages are defined as

$$\begin{cases} v'_a = 0 \\ v'_b = M \sin\left(2\pi f_o t - \dfrac{5\pi}{6}\right) \\ v'_c = M \sin\left(2\pi f_o t + \dfrac{5\pi}{6}\right), \end{cases} \tag{6}$$

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where, M and f_o are the modulation index and the output frequency, respectively.

In Fig. 4(a), control signals of S_{1b}, S_{2b}, and S_{3b} are produced by comparing the reference voltages ± with high-frequency carrier v_{car1}, whereas the control signals of S_{1c}, S_{2c}, and S_{3c} are created by comparing the reference voltages ± with v_{car1}. Note that switch S_{2a} is fully turned on, while switches S_{1a}, and S_{3a} are fully turned off when the fault occurs in phase-A. The ST signal of the T-type inverter is generated by comparing two constant voltages V_{SH} and $-V_{SH}$ with v_{car1}. Constant voltages V_{con1} and V_{con2} are compared with other high-frequency carrier v_{car2} to generate the control signals for switches T_1 and T_2, respectively. It is worth noting that V_{con1} and V_{con2} are limited to $[1-\hat{V}_{SH}, \hat{V}_{SH}]$ and $[-\hat{V}_{SH}, \hat{V}_{SH}-1]$ respectively, where $\hat{V}_{SH}$ is the amplitude of V_{SH}.

Fig. 4(b) shows the PWM control method for the fault-tolerant TL qSBT^{2}I when a fault occurs in T_1 of AIS network. The reference voltages of the inverter are compared with v_{car1} to create the control signals for S_{1x}, S_{2x}, and S_{3x}. The ST control signal of the T-type inverter is produced by comparing two constant voltages V_{ST} and $-V_{ST}$ with V_{car1}. The control signal of switch T_2 is created by comparing two constant voltages V_{SH} and $-V_{SH}$ with V_{car2}.

Like the PWM control method for TL qSBT^{2}I in [17], the proposed PWM control methods for the fault-tolerant TL qSBT^{2}I benefits from low input current ripple because the inductor has four cycles of energy store-release within a switching period. Although other ST control strategies can be used for the optimization of the fault-tolerant TL qSBT^{2}I, its input current ripple will be increased owing to the use of variable ST duty cycle.

D. Steady-State Analysis for the Fault-Tolerant TL qSBT^{2}I When T-Type Inverter Switch is Faulty

In Fig. 4(a), $(d- D_0)\cdot T/2$ is the total time interval of NST modes 1 and 2 where d is the duty cycle of the switches T_1 and T_2 and is controlled by V_{con1} and V_{con2}. The time interval of both ST and NST 3 cases is $D_0\cdot T$. Consequently, the time interval of the NST 4 case is $(1 - D_0 - d)\cdot T$. Supposing capacitors C_1 and C_2 are large enough to maintain a ripple-free voltage across the capacitors and that a capacitor voltage balance controller [17] is applied to the fault-tolerant TL qSBT^{2}I, then $V_{C1} = V_{C2} = V_C$.

Applying volt-second balance principle in steady state equilibrium across the inductor and the charge-second balance principle in steady state equilibrium across the capacitors, and from (1) to (5), the capacitor voltages V_{C1} and V_{C2} are found to be,

$$V_C = V_{C1} = V_{C2} = \frac{V_g}{2-3D_0-d} \tag{7}$$

The peak output phase voltage is found as,

$$\hat{v}_x = \frac{M\cdot V_{PN}}{2} = M\cdot V_C = \frac{M}{2-3D_0-d}V_g. \tag{8}$$

The boost factor, B of the fault-tolerant TL qSBT^{2}I is determined as

$$B = \frac{V_{PN}}{V_g} = \frac{2V_C}{V_g} = \frac{2}{2-3D_0-d}. \tag{9}$$

E. *Steady-State Analysis for the Fault-Tolerant TL qSBT^{2}I When* AIS *Switch is Faulty*

When an OCS T_1 fault occurs, the fault-tolerant TL qSBT^{2}I has two additional NST states as shown in Figs. 2(c) and 2(d) besides the ST state. To maintain the output voltage at per-fault, node P should be connected to node O directly. Then, the inverter operates with a new DC-link between nodes O and N to generate a two-level output voltage. When switches S_{1a} and S_{2a} are switched "ON" to connect P with O, the output phase-A voltage is zero. If switch S_{1x} or S_{2x} ($x = b$ or c) is switched "ON", the output phase-B or phase-C voltage is zero. If switch S_{3b} or S_{3c} is switched "ON", the output phase phase-B or phase-C voltage is $-V_{C2}$. In NST 5 mode as shown in Fig. 2(c), switch T_2 is switched "ON" during the time interval of $D_0\cdot T$. Inductor L_B stores energy and the inductor voltage is defined in (3).

In NST 6 mode as shown in Fig. 2(d), switch T_2 is switched "OFF". Inductor L_B releases energy and the inductor voltage is defined in (1). The time interval in this state is $(1 - 2D_0)\cdot T$.

In ST mode, the T-type inverter switches are switched "ON" at the same time, while switch T_2 is switched "OFF" during the time interval of $D_0\cdot T$. Inductor L_B stores energy and the inductor voltage is defined in (5).

Applying volt-second balance principle to inductor L_B, capacitor C_2 voltage is expressed as in (10) in steady state

$$V_{C2} = \frac{V_g}{1-2D_0} \tag{10}$$

The peak output phase voltage is

$$\hat{v}_x = M\cdot V_{ON} = M\cdot V_{C2} = \frac{M}{1-2D_0}V_g. \tag{11}$$

III. Fault-Tolerant Control Scheme for TL qSBT^{2}I.

When an OCS fault occurs in switch S_{1a} or S_{3a}, the inverter can generate the two-level output voltage after reconfiguring the topology and modulation. As a result, the output phase voltage is reduced by $1/\sqrt{3}$ times compared to the normal operation mode. In this case, the output voltage amplitude of the fault-tolerant TL qSBT^{2}I must be compensated by either increasing the modulation index or changing the ST duty ratio. However, the increase of either the modulation index or ST duty cycle should correlate with the output phase voltage reduction of $\sqrt{3}$. Concerning the control parameters of the fault-tolerant TL qSBT^{2}I, the increase of the output voltage amplitude can be obtained by (8). To compensate the amplitude reduction of the faulty phase, a variation in three control parameters M, D_0, and d is required.

Fig. 5 shows the flow chart of the proposed control method for the fault-tolerant TL qSBT^{2}I. The flowchart can be explained as follows. The input and output voltages are entered to calculate the desired voltage gain of the inverter in the normal and faulty modes as

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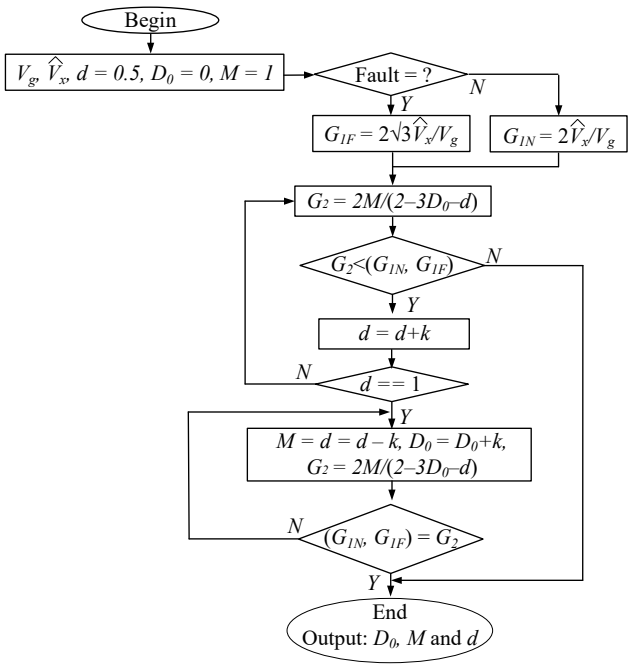

Fig. 5. Flow chart of the proposed control method before and after S_{1a} fault.

$$\begin{cases} G_{1N} = \dfrac{2\hat{v}_x}{V_g} \ \text{in normal mode} \\ G_{1F} = \dfrac{2\sqrt{3}\hat{v}_x}{V_g} \ \text{in faulty mode} \end{cases} \tag{12}$$

The proposed control scheme is designed such that it gives a priority to keep M as high as possible. Thus, the initial values of the modulation index and ST duty cycle are set to $M = 1$ and $D_0 = 0$. To boost the voltage, the duty cycle of the switches in AIS, d is set to be 0.5 and that is based on the minimum voltage gain required in the fault-tolerant TL qSBT^{2}I. Then, the calculated voltage gain, G_2, is determined as

$$G_2 = \frac{2M}{2-3D_0-d} \tag{13}$$

Next, the desired value G_{1N} in the normal mode or G_{1F} in the fault mode is compared with G_2. If G_2 is lower than G_{1N} or G_{1F}, duty cycle d of the switches in AIS will be increased with a step number of k until d reaches 1. It is worth noting that k is a fraction. If k is selected to be too small, the calculated values of the duty cycles and modulation index become finer while the calculation time is longer. Therefore, a trade-off is made with the selection of step k in the proposed method to be 0.01. When $d = 1$ and G_2 is still smaller than G_{1N} or G_{1F}, D_0 is increased in steps of k while M and d are decreased in steps of k. The value of G_2 can then be recalculated as in (13). The comparison will be repeated until G_2 is larger than G_{1N} or G_{1F} and the flowchart will end with gathering the optimal output control parameters of D_0, M, and d.

IV. Comparative Study

In this section, the proposed PWM scheme for the fault-tolerant TL qSBT^{2}I is compared to PWM method of fault-tolerant impedance source inverters described in [26], [27]. As compared in [17], the TL qSBT^{2}I uses less passive elements and more active components than TL qZST^{2}I in [26]. Moreover, the input current ripple of the TL qSBT^{2}I under the proposed PWM scheme is reduced in comparison to that under the PWM method in [26], [27]. Therefore, the size and weight of the fault-tolerant TL qSBT^{2}I are lower than those of the fault-tolerant TL qZST^{2}I in [26].

In the PWM method for fault-tolerant impedance source inverters [26], [27], the voltage gain is controlled by the modulation index, M and ST duty cycle, D_0. However, M is limited by $(1 - D_0)$. When the impedance source inverters [26][27] operate in the faulty mode, low M and high D_0 must be used to maintain the output voltage at its pre-fault value. Because of using low M and high D_0, the output quality of the inverter is low and the power loss of the inverter is increased owing to high shoot-through current. Moreover, a voltage stress of the semiconductors is increased because the DC-link voltage is high with low M. The voltage gain of the fault-tolerant three-level impedance source inverters with the modulation method in [26] and [27] is given as

$$G = \frac{\hat{v}_x}{V_g/2} = \frac{M}{1-2D_0}. \tag{14}$$

Under the proposed modulation scheme, a low shoot-through duty cycle is made a priority so that the selected M is kept as high as possible. Thus, the initial values of the modulation index and ST duty cycle are set to $M = 1$ and $D_0 = 0$. To boost the voltage, the duty cycle of the switches in AIS network, d is set to be 0.5. Then, a flow chart of the control scheme as shown in Fig. 5 is employed. As a result, optimal values for M, D_0, and d are achieved. The voltage gain of the fault-tolerant three-level qSBT^{2}I with the proposed modulation scheme is derived from (8) as

$$G = \frac{\hat{v}_x}{V_g/2} = \frac{M}{1-2D_0}. \tag{15}$$

A minimum value of d is set to 0.5 in the proposed method for the fault-tolerant three-level qSBT^{2}I. Substituting $d = 0.5$ and $D_0 = 1 – M$ into (14) and (15), the voltage gain of the fault-tolerant three-level inverters is rewritten as

$$\begin{cases} G = \dfrac{M}{2M-1} \ \text{method in [26][27]} \\ G = \dfrac{2M}{3M-1.5} \ \text{proposed method.} \end{cases} \tag{16}$$

Fig. 6 shows the voltage gain comparison for the method in [26][27] and the proposed method for the fault-tolerant three-level qSBT^{2}I. As shown in Fig. 6, the proposed method uses a higher modulation index to generate the same voltage gain in comparison to the method in [26][27]. As a result of using a high modulation index, the fault-tolerant three-level qSBT^{2}I with the proposed method has a lower DC-link voltage. It is worth noting that the voltage gain of the fault-tolerant three-level qSBT^{2}I in Fig. 6 is kept at the minimum value corresponds

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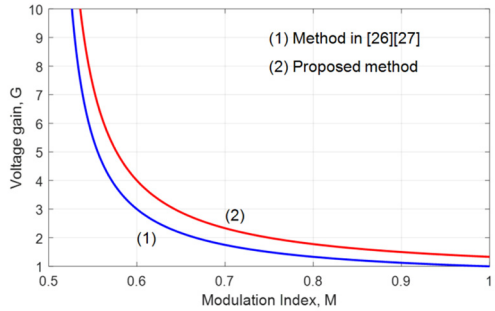

Fig. 6. Voltage gain comparison between the method in [26], [27] and the proposed method for the fault-tolerant three-level qSBT^{2}I.

to d = 0.5. When the proposed method is applied to the fault-tolerant three-level qSBT^{2}I by selecting appropriate parameters of M, D_0, and d, the voltage gain of fault-tolerant three-level qSBT^{2}I will be higher than red line (or line 2) in Fig. 6.

When an OCS fault occurs, a high boost voltage is required to maintain the output voltage at its pre-fault value. Consequently, the capacitors and DC-link voltages are increased to compensate the voltage of the faulty phase. This issue is also found in the three-level impedance source inverters in [26][27]. However, the voltage stress on the switches and capacitors of the fault-tolerant three-level qSBT^{2}I with the proposed method is still lower than that of the methods described in [26][27] owing to using a high modulation index as seen in Fig. 6.

When compared with the conventional fault-tolerant T-type inverter, the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme has the following advantages. Unlike the conventional fault-tolerant T-type inverter, the fault-tolerant TL qSBT^{2}I tolerates the ST phenomenon because of the impedance source network. As a result, the power semiconductor devices of the fault-tolerant TL qSBT^{2}I are safe for a certain time that is enough to shut down the system when a DC-link short circuit occurs. Therefore, the dead-time between the upper and lower switches of the each inverter leg is not necessary and can be removed from the fault-tolerant TL qSBT^{2}I. Consequently, the output quality of the fault-tolerant TL qSBT^{2}I is improved. Moreover, the fault-tolerant TL qSBT^{2}I has a buck-boost voltage ability that can be effectively used to compensate the reduced voltage of the faulty phase and maintain a constant output voltage at its pre-fault value.

V. Simulation and Experimental Results

A. Simulation Results

To verify the performance of the fault-tolerant TL qSBT^{2}I, PSIM simulation studies are performed. The circuit parameters are listed in Table III. Figs. 7-9 show the simulation results of the fault-tolerant TL qSBT^{2}I before and after failure of S_{1a} when V_{dc} = 165 V. Under healthy conditions, the capacitors C_1 and C_2 voltages are boosted to the same value of 181 V and the DC-link voltage is 362 V. When a fault in switch S_{1a} occurs, by reconfiguring the circuit, the capacitors and DC-link voltages before and after S_{1a} fault are kept unchanged as shown Fig. 7(a). However, phase-A voltage is decreased by √3 times. To

TABLE III
Parameters Used in Simulation and Experiments

Parameter/ Component		Value
Power rating	P_o	1 kW
Input voltage	V_g	165 V
Desired output phase voltage	V_{XG}	110 Vrms
Output frequency	f_o	50 Hz
Carrier frequency	f_s	5 kHz
Boost inductor	L_B	3 mH/ 20 A, 0.12 Ω
Capacitors	$C_1 = C_2$	2200 μF, 44 mΩ
Three-phase LC filter	L_f and C_f	3 mH and 10 μF
Three-phase resistive load	R_{load}	40 Ω
DSEI60-12A Diodes	$D_1 - D_4$	1200 V, 52 A
FGL40N150D IGBTs	S_{1x}–S_{3x}, T_1, T_2	1500 V, 40 A

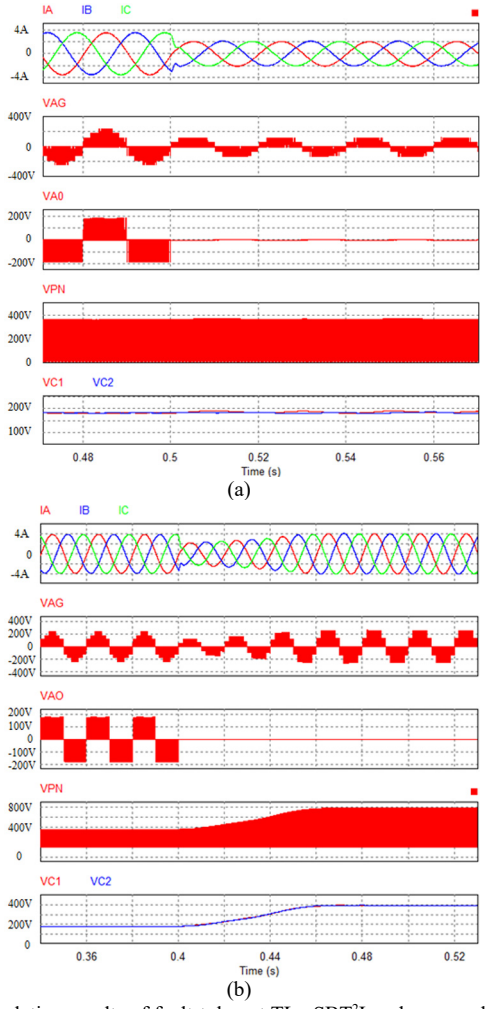

Fig. 7. Simulation results of fault-tolerant TL qSBT^{2}I under normal and OCS S_{1a} fault conditions with (a) only reconstructing the topology and (b) both reconstructing the topology and compensating voltage by changing control parameters.

compensate the output voltage reduction, the proposed scheme is applied to the fault-tolerant TL qSBT^{2}I where capacitor C_1 and C_2 voltages are boosted to 381 V after S_{1a} fault as shown in Fig. 7(b). The DC-link voltage before and after the faulty condition is 381 V and 762 V, respectively. The output current is balanced and recovered. In normal mode, the pole voltage (V_{AO}) has three levels: 181 V, 0 V, and −181 V.

Fig. 8 shows the simulation results of the fault-tolerant TL qSBT^{2}I when switch S_{2a} is faulty in OCS. In this case, the

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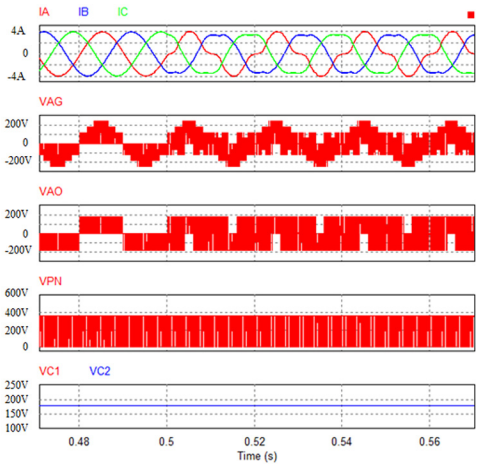
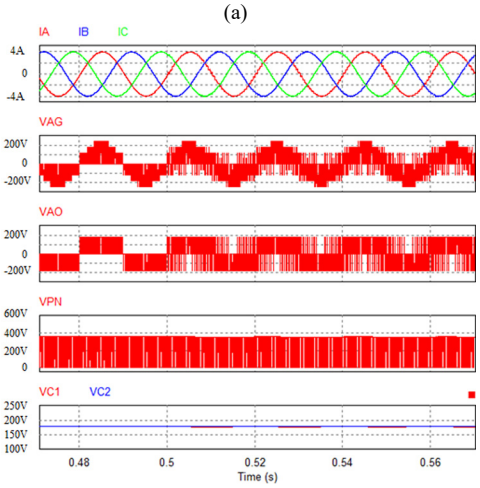


(a)



(b)

Fig. 8. Simulation results of fault-tolerant TL qSBT^{2}I under normal and OCS S_{2a} fault mode (a) without and (b) with the proposed modulation strategy.

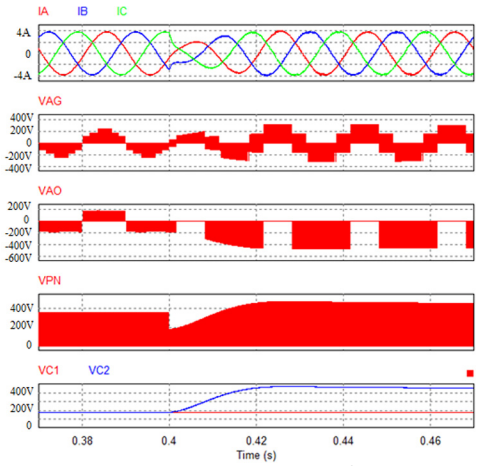
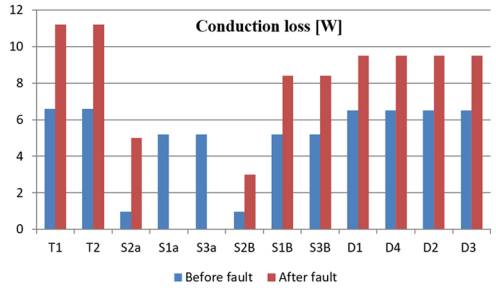
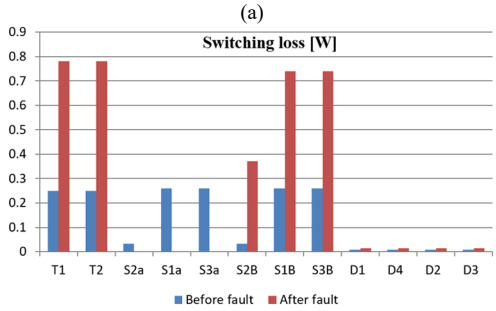


Fig. 9. Simulation results of fault-tolerant TL qSBT^{2}I under normal and OCS T_1 fault conditions with the proposed modulation scheme.

voltage of phase-A has two levels. As a result, the output load current is distorted when there is no change in modulation but the system is still able to operate as shown in Fig. 8(a). Fig. 8(b) shows the results of the system when the proposed modulation scheme is applied after the fault. Consequently, the distortion of the load currents is removed perfectly.



(a)



(b)

Fig. 10. Simulated (a) conduction and (b) switching losses of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme before and after an OCS S_{1a} fault.

Fig. 9 shows the simulation results of the fault-tolerant TL qSBT^{2}I when switch T_1 of AIS network has an OCS fault. To compensate the output voltage reduction, the proposed modulation scheme is applied to the fault-tolerant TL qSBT^{2}I as shown in Fig. 9 where the capacitor C_1 voltage is held constant at 181 V, while the capacitor C_2 voltage is boosted to 458 V after the OCS T_1 fault. The output phase voltage has two levels. The peak DC-link voltage before and after the faulty condition is 362 V and 458 V, respectively. The output current is balanced and recovered.

Fig. 10 shows simulated conduction and switching losses of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme before and after an OCS S_{1a} fault. Note that the power loss of switches S_{1c}, S_{2c}, and $S_{3}c$ is the same to that of S_{1b}, S_{2b}, and S_{3b} as shown in Fig. 10. Total power losses before and after fault at 900 W output power are 75.5 W and 110.32 W, respectively. Therefore, the efficiency of the inverter before and after fault is 92.3% and 89.1%, respectively. The increment in power loss in the fault duration is due to the increased boost during the ST period that gives rise to higher transistor conduction losses. The efficiency could have been improved further, had the diodes and transistors been selected optimally for this application. However, authors had to contend with the devices that are available in the laboratory during the implementation phase of this study.

B. Experimental Results

A 1 kW prototype was constructed to demonstrate the operating principle of the fault-tolerant TL qSBT^{2}I. Fig. 11 shows a photo of the hardware setup. In order to detect the fault, LEM-LA 25-P current transducers are used to measure output current signals. When one of the switches undergoes an OCS fault, the current sensors will update the changed output currents for the control system to handle the fault. As numerous

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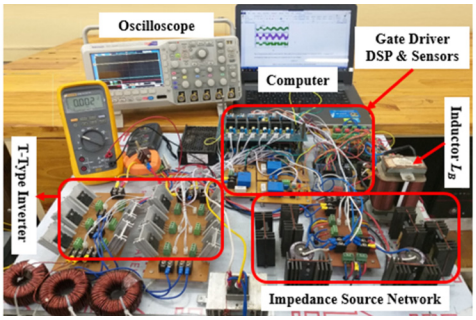

Fig. 11. A photo of the hardware setup.

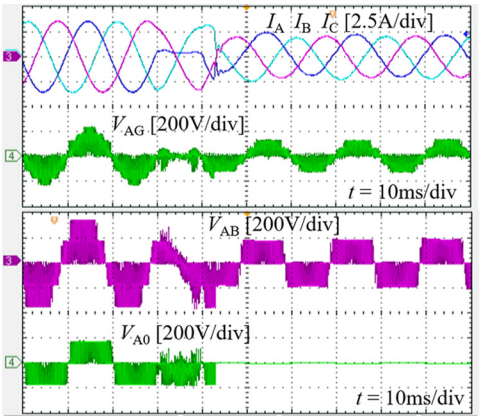

Fig. 12. Experimental results under normal and OCS S_{1a} fault conditions with reconstructing topology.

fault detection schemes have been reported in the literature [31], [32], it has not been investigated in this study.

Figs. 12-18 show the experimental results of the fault-tolerant TL qSBT^{2}I under different working conditions. In Figs. 12, 13(c), 14, 15(b), and 16(b), the waveforms from top to bottom are the output phase currents (I_A, I_B, I_C), the output phase voltage (V_{AG}), the output line-to-line voltage (V_{AB}), and the pole voltage (V_{A0}). Fig. 12 shows the experimental results of the fault-tolerant TL qSBT^{2}I when an OCS S_{1a} fault occurs. After the OCS S_{1a} fault occurrence, the load current is asymmetrical and distorted if the modulation technique is not applied. After reconfiguring the circuit and modulation, the output current of the inverter is balanced as shown in Fig. 12. However, its amplitude is decreased as compared with the normal operation mode because the boost voltage control is not applied.

Fig. 13 indicates the experimental results of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme when an OCS S_{1a} fault occurs, where a full modulation technique with reconfigurating circuit and compensating voltage are employed. Under normal conditions, TL pole voltage (V_{A0}) has three levels: 176 V, 0 V, and -176 V. The simulated values are higher than the measured values because the voltage drops across the devices are neglected in the simulations. From Fig. 13(b), it is possible to see that the capacitor and DC-link voltages are boosted to 176 V and 368 V respectively from 165 V input voltage in the normal mode. When switch S_{1a} is failed, the capacitor and DC-link voltages are boosted to 368 V and 736 V respectively to compensate the voltage of the faulty phase. It is worth noting that the voltage rating of capacitors and blocking

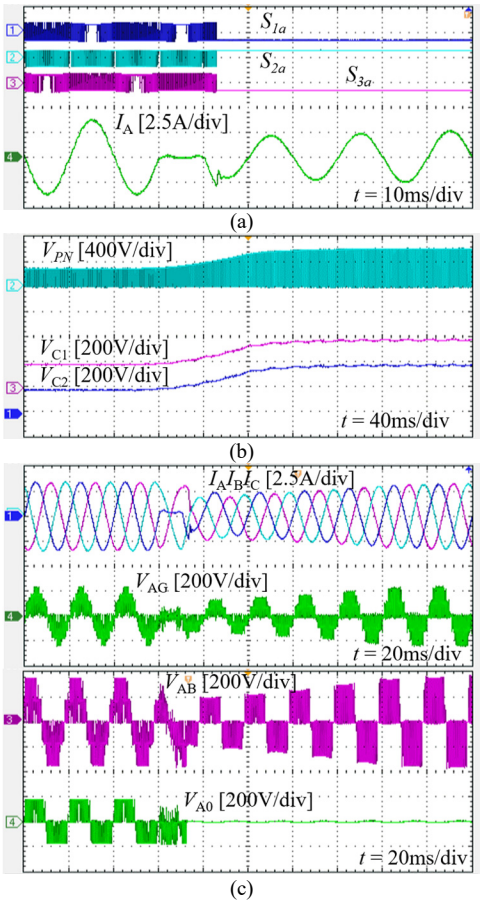

Fig. 13. Experimental results under normal and OCS S_{1a} fault conditions with reconstructing topology and compensating voltage. (a) Leg-A switch control signals, (b) DC-link and capacitor voltages, and (c) output side waveforms.

voltage of the switches in the fault-tolerant TL qSBT^{2}I need to be doubled with the proposed PWM scheme in comparison to those under normal operation conditions. This problem is also found in the conventional fault-tolerant TL inverter topologies where additional phase legs or branches and/or switches are not used. As shown in Fig. 13(c), the amplitudes of load currents and voltages of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme are effectively recovered to their pre-fault values.

Figs. 14 and 15 show the experimental waveforms of the fault-tolerant TL qSBT^{2}I under switch S_{2a} fault condition. The load currents and output phase voltages are distorted as shown in Fig. 14. The TL pole voltages are affected when compared to those under normal conditions. The waveforms in Fig. 15(a) show gating control signal for phase-A and load current before and after fault. The waveforms in Fig. 15(b) show that the compensation scheme under the fault condition helps to maintain the output waveforms as in the normal condition. In this situation, the distortion of the output currents can also be mitigated in this failure mode.

Fig. 16 shows the experimental waveforms of the fault-tolerant TL qSBT^{2}I-UFM with the proposed PWM scheme under OCS T_1 fault condition. From Fig. 16(a), it is possible to see that in the normal condition, the capacitor and DC-link

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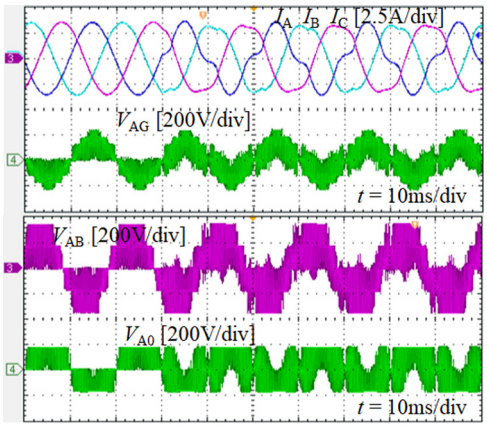

Fig. 14. Experimental results in normal and OCS fault mode of the S_{2a} without using the proposed modulation strategy.

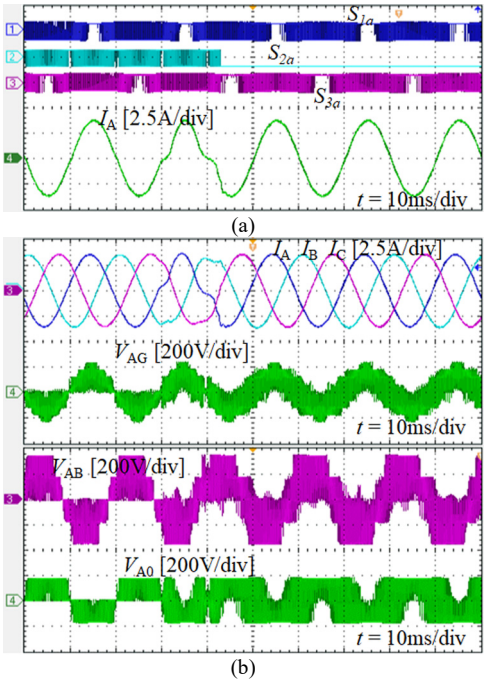

Fig. 15. Experimental results in normal and OCS fault mode of the S_{2a} with the proposed modulation strategy. (a) Control signals and (b) output side waveforms.

TABLE IV
THD OF LOAD CURRENT AND VOLTAGE IN NORMAL AND FAULT CONDITIONS

Condition	Method in [27]		Proposed method	
	THDi	THDv	THDi	THDv
Normal	3.19%	70.1%	2.77%	62.42%
S_{1a} fault with reconfiguration circuit	5.38%	119.8%	4.58%	91.68%
S_{2a} fault with changing modulation scheme	4.74%	125.8%	3.37%	86.96%
T_1 fault with reconfiguration circuit	NA	NA	4.43%	119.8%

voltages are boosted to 176 V and 348 V, respectively. When switch S_{1a} is failed, the capacitor C_2 and DC-link voltages are boosted to 436 V, while the capacitor C_1 voltage is unchanged. As shown in Fig. 16(b), the amplitude of load currents is recovered in pre-fault value.

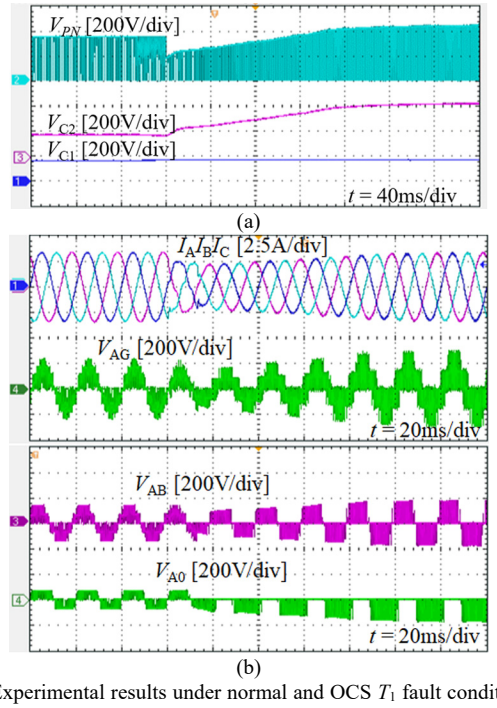

Fig. 16. Experimental results under normal and OCS T_1 fault conditions with the proposed PWM scheme. (a) DC-link and capacitor voltages and (b) output side waveforms.

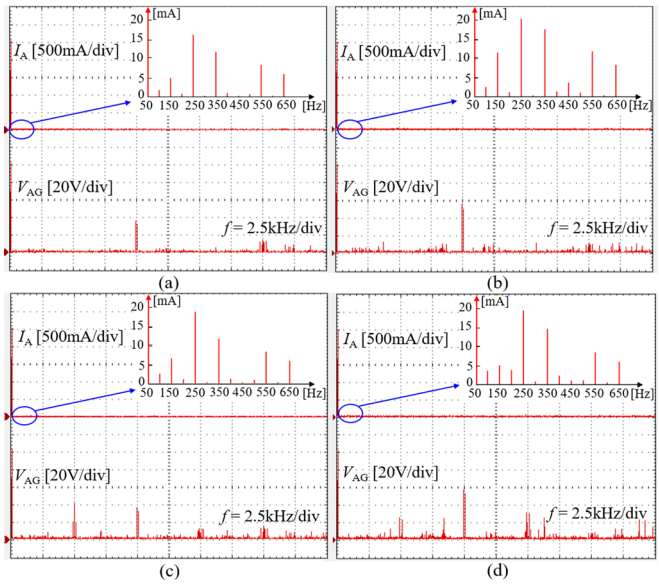

Fig. 17. Harmonic spectrum of load current and phase voltage (a) under normal conditions, (b) after OCS S1a fault with reconfiguration circuit and compensation voltage, (c) after OCS S_{2a} fault with the proposed PWM strategy, and (d) after OCS T_1 fault with the proposed PWM strategy.

Fig. 17 shows the harmonics spectrum of the output voltage and current of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme at different operating conditions. Table IV compares THD values of the output current and voltage between the proposed scheme and the PWM method described in [27] for the fault-tolerant TL qSBT^{2}I. Under normal conditions, THD values of the load current (THDi) and phase voltage (THDv) with the propsoed PWM scheme are 2.77% and 62.42%, while they are 3.19% and 70.1% with the PWM method in [27], respectively. When an OCS fault occurs, both

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2922687, IEEE Journal of Emerging and Selected Topics in Power Electronics

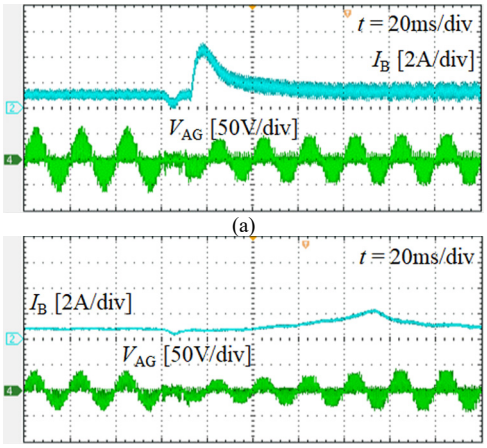

Fig. 18. Experimental results of transient-current for fault-tolerant TL qSBT^{2}I under normal and OCS S_{1a} fault conditions at input voltage of 30V with (a) the PWM method in [27] and (b) the proposed PWM scheme.

THDi and THDv with the propsoed PWM scheme are increased, but still lower than that of the method given in [27]. As shown in Figs. 17(c) and 17(d), the harmonics at the switching frequency of 5 kHz of the phase voltage only appear when an OCS S_{2a} fault occurs. This is because the output phase-A voltage has two levels. As shown in Fig. 17, the amplitude of the current spectra at low frequency is too small in comparison to that at the fundamental frequency of 50 Hz.

Fig. 18 shows a transient-current comparison for the fault-tolerant TL qSBT^{2}I between the PWM method in [27] and the proposed scheme for the same voltage gain condition. For safety reasons, a low input voltage of 30 V is used to reduce the transient current of the fault-tolerant TL qSBT^{2}I. As shown in Fig. 18(a), the peak inductor current with the PWM method in [27] is 4.5 A, while it is 2.1 A with the proposed scheme. Moreover, a low inductor current ripple and a low peak output voltage are evident in the the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme resulting in reduced voltage stress across the power devices in the inverter.

VI. Conclusion

This paper presents a novel fault-tolerant TL qSBT^{2}I and its PWM control strategy. The main properties of the fault-tolerant TL qSBT^{2}I with the proposed PWM method are as follows: 1) improved THD of the current in comparison with that in [27], 2) improved control parameters in comparison with the works in [26], [27] 3) ability to operate in normal and fault modes, and 4) reduced voltage stress in power semiconductors in comparison with the method in [27]. The steady state analysis, operating principles in fault modes, and simulation results of the fault-tolerant TL qSBT^{2}I are shown. A new operating condition under OCS fault in AIS network is investigated. Moreover, a comparative analysis between the fault-tolerant TL qSBT^{2}I with the proposed PWM method and the conventional fault-tolerant T-type inverters is presented. A laboratory prototype is built to verify the operating principles of the fault-tolerant TL qSBT^{2}I with the proposed PWM scheme. Simulations and experimental results confirm the theoretical analysis. The fault-tolerant TL qSBT^{2}I with the proposed PWM method is well suited for low and medium power renewable energy applications where the system availability, safety, and reliability are paramount. However, for fault tolerant inverter designs, the efficiency is not the most important measure of the system but the reliability and availability are.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2922687, IEEE Journal of Emerging and Selected Topics in Power Electronics

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Duc-Tri Do was born in Vietnam in 1973. He received the B.S. and M.S. degrees in electronic engineering from the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam, in 1999 and 2012, respectively. He is currently a Lecturer with the Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education. His current research interests include power converters for renewable energy systems.

Minh-Khai Nguyen (S'09–M'12–SM'18) received the B.S. degree in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2005, and the M.S. and Ph.D. degrees in electrical engineering from Chonnam National University, Gwangju, South Korea, in 2007 and 2010, respectively. He was a Lecturer with the Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, and an Assistant Professor with Chosun University, Gwangju, South Korea. He is currently with the School of Electrical Engineering and Computer Science, Queensland University of Technology, Australia. His current research interests include impedance-source inverters and power converters for renewable energy systems. He had served as a Guest Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS special issue on the impedance source converter topologies and applications. He is currently an Associate Editor for the Journal of Power Electronics.

Quach Thanh Hai was born in 1972, in Vietnam. He received B.S degrees in Electrical Engineering from Ho Chi Minh City University of Technology and Education, Vietnam, in 1995 MS and PhD degrees in Electrical Engineering from Ho Chi Minh City University of Technology, Vietnam, in 2002 and 2014. Since 1995, he has been with the Department of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Vietnam. His research interests are power electronics and PWM techniques.

Vinh-Thanh Tran was born in Viet Nam, in 1995. He received the B.S. degree in Electronic Engineering from Ho Chi Minh City University of Technology and Education, Viet Nam, in 2018. He currently working toward the M.S. degree in Electronic Engineering from Ho Chi Minh City University of Technology and Education, Viet Nam. His current research interests include impedance source inverter and control of multi-level inverter.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications. He has received 30 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

D. Mahinda Vilathgamuwa (S'90–M'93–SM'99) received the B.Sc. degree in electrical engineering from the University of Moratuwa, Moratuwa, Sri Lanka, in 1985, and the Ph.D. degree in electrical engineering from Cambridge University, Cambridge, U.K., in 1993. He joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 1993. He is currently a Professor of power engineering with the Queensland University of Technology, Brisbane, QLD, Australia. He has published over 275 research papers in refereed journals and conferences. His research interests include wireless power, battery storage, power electronic converters, electrical drives, and electromobility.

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